

**METHOD AND APPARATUS FOR FAULT-TOLERANCE VIA DUAL
THREAD CROSSCHECKING**



ABSTRACT

A method (and structure) of concurrent fault crosschecking in a computer having a plurality of simultaneous multithreading (SMT) processors, each SMT processor simultaneously processing a plurality of threads, includes processing a first foreground thread and a first background thread on a first SMT processor and processing a second foreground thread and a second background thread on a second SMT processor. The first background thread executes a check on the second foreground thread and the second background thread executes a check on the first foreground thread, thereby achieving a crosschecking of the execution of the threads on the processors.

YOR920010219US2